

**SGS-THOMSON ASIC DESIGN KITS**

Type	Description
Cadence ASIC Design Kit (ADK)	SUN based. Includes support for Verilog, Veritime, Verifault. Delay calculator with RC-backannotation. Module Generators. EWS interface. ATE support to testers. Synopsys interface. Preview interface. Bonding diagram manager. VHDL simulation (LEAPFROG). Clock tree synthesis. Qualified as Golden System.
Mentor ASIC Design Kit (MDK)	SUN and HP based. Includes support for Quicksim, Quickpath, Quickgrade. Delay calculator with RC - backannotation. Module generators. ATE support to testers. Synopsys and Autologic interface. VHDL simulation (QUICKVHDL). Clock tree synthesis. Qualified as Golden System.
Synopsys Synthesis Design Kit	Logic Synthesis including Design Compiler, Design Analyzer and Test Compiler. Available on SUN and HP platforms. Mentor, Cadence and Verilog interfaces.
Verilog Stand alone Simulator Design Kit	Available on SUN platform.
System HILO Stand alone Simulator Design Kit	Available on SUN, HP and DEC platforms.
Synopsys V <sub>SS</sub> Stand alone Simulator Design Kit	Available on SUN and HP platforms.