SGS-THOMSON MICROELECTRONICS

ST486DX/DX2

5 Volt CPUs

PRELIMINARY DATA

IMPROVED 486DX/DX2 PERFORMANCE

- Clock doubled core speeds up to 80 MHz
- Integrated FPU 10% faster than 80486DX
- Up to 50 MHz bus speeds for fast local bus systems

INDUSTRY STANDARD 486 COMPATIBILITY

- 486DX socket and instruction set compatible
- Runs DOS, Windows, OS/2, UNIX
- Standard 168-pin PGA

ON-CHIP 8-KBYTE WRITE-BACK CACHE

- Up to 15% higher performance than write-through (PC Bench 8.0, 80MHZ)
- Industry-wide write-back chipset suppor
- Burst-mode write capability
- Configurable as write-back or write-through

ADVANCED POWER MANAGEMENT

- Fast SMI interrupt with separate memory space
- Fully static design permits dynamic clock control
- Software or hardware initiated low power suspend
- Automatic FPU power-down mode

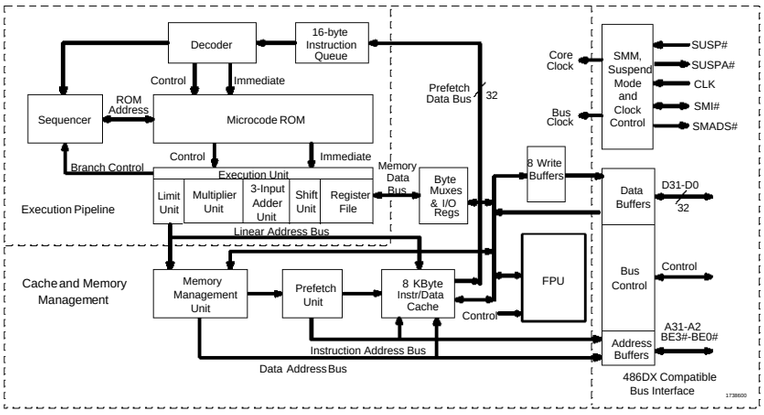
The SGS-THOMSON ST486DX/DX2 5 volt CPUs are advanced 486DX/DX2 compatible processors. These CPUs incorporate an on-chip 8KByte write-back cache and an integrated math coprocessor.

The on-chip write-back cache allows up to 15% higher performance by eliminating unnecessary external write cycles. On traditional write-through CPUs, these external write cycles can create bus bottlenecks affecting system wide performance.

The integrated floating point unit, improves performance up to 10% over the 80486DX as measured using Power Meter Whetstone test.

These processors are designed to meet the power management requirements in the newest generation of low-power desktops and notebooks. Power is saved by taking advantage of advanced power management features such as static circuitry, SMM, and automatic FPU power-down. Fast entry and exit of SMM allows frequent use of the SMM feature without noticeable performance degradation.

This CPU family maintains compatibility with the installed base of x86 software and provides essential socket compatibility with the 486DX/DX2



1.0 PRODUCT OVERVIEW

The SGS THOMSON ST486DX™ 5-volt microprocessors are advanced 486DX/DX2 microprocessors. The ST486DX CPU operates at the same speed as the external bus and the ST486DX2 CPU operates at twice the external bus speed. The "ST486DX/DX2" designation refers to either the ST486DX or ST486DX2 microprocessor. A more complete product description can be found in the SGS-Thomson ST486DX/DX2 data book. (see ordering instructions).

The CPUs in the ST486DX/DX2 family are high speed 5-volt CPUs attaining clock-doubled core speeds of up to 80 MHz.

The ST486DX/DX2 8-KByte cache can be configured to run in traditional write-through mode or in the higher performance write-back mode. Write-back mode eliminates unnecessary external memory write cycles offering up to 15% higher overall performance (80 MHz, PC Bench 8.0) than write-through mode.

The ST486DX/DX2 supports 8, 16 and 32-bit data types and operates in real, virtual 8086 and protected modes. The CPU can access up to 4 GBytes of physical memory using a 32-bit burst mode bus. Floating point instructions are parallel processed using an on-chip math coprocessor.

The ST486DX/DX2 CPUs are ideal design solutions for low-powered "Green PC" desktops as well as portable computers. These microprocessors typically draw only 450 µA, while the input clock is stopped in suspend mode, due to their static design. System Management Mode (SMM) allows the implementation of transparent system power management or the software emulation of I/O peripheral devices.

A list of ST486DX/DX2 5-volt parts, including their operating frequency, and package types are listed on page 12 of this document.

1.1 Clock-Doubled CPU Core

The clock-doubled ST486DX2 CPU core operates at twice the frequency of the external clock input, while continuing to operate the bus interface at the external clock frequency. This configuration provides high frequency CPU performance without requiring a high speed interface to external memory.

The ST486DX2 provides up to 1.8 times the performance of a 486DX at the same external clock frequency. This level of performance is achieved by doubling the frequency of the input clock and using the resulting signal to drive the CPU core. To further enhance this architecture, the ST486DX2 reduces the performance penalty of slow external memory accesses through use of an on-chip write-back cache and eight write buffers.

The CPU core consists of a five-stage pipeline optimized for minimal instruction cycle times and includes all necessary hardware interlocks to permit successive instruction execution overlap. The execution stage of the pipeline executes simple but frequently used instructions in a single clock cycle and the hardware multiplier executes 16-bit integer multiplies in only three clocks.

1.2 On-Chip Write-Back Cache

The ST486DX/DX2 on-chip cache can be configured to run in traditional write-through mode or in a higher performance write-back mode. The write-back cache mode was specifically designed to optimize performance of the CPU core by eliminating bus bottlenecks caused by unnecessary external write cycles. This write-back architecture is especially effec-

tive in improving performance of the clock-doubled ST486DX2 CPU.

Traditional write-through cache architectures require that all writes to the cache also update external memory simultaneously. These unnecessary write cycles create bottlenecks which result in CPU stalls and adversely impact performance. In contrast, a write-back architecture allows data to be written to the cache without updating external memory. With a write-back cache, external write cycles are only required when a cache miss occurs, a modified line is replaced in the cache, or when an external bus master requires access to data.

The ST486DX/DX2 cache is an 8-KByte unified instruction and data cache implemented using a four-way set associative architecture and a least recently used (LRU) replacement algorithm. The cache is designed for optimum performance in write-back mode, however, the cache can be operated in write-through mode. The cache line size is 16 bytes and new lines are only allocated during memory read cycles. Valid status is maintained on a 16-byte cache line basis, but modified or "dirty" status for write-back mode is maintained on a 4-byte (double-word) basis. Therefore, only the double-words that have been modified are written back to external memory when a line is replaced in the cache. The CPU core can access the cache in a single internal clock cycle for both reads and writes.

1.3 FPU Operations

Since the FPU is resident within the CPU, the overhead associated with external math coprocessor cycles is eliminated. If the FPU is not in use, the FPU is automatically powered down. This feature reduces overall power consumption. The integrated FPU results in the addition of two new pins FERR# (replaces ERROR#) and IGNNE#.

1.4 System Management Mode

System Management Mode (SMM) provides an additional interrupt and a separate address space that can be used for system power management or software transparent emulation of I/O peripherals. SMM is entered using the System Management Interrupt (SMI#) or SMINT instruction. While running in isolated SMM address space, the SMI interrupt routine can execute without interfering with the operating system or application programs.

After entering SMM, portions of the CPU state are automatically saved. Program execution begins at the base of SMM address space. The location and size of the SMM memory are programmable within the ST486DX/DX2. Eight SMM instructions have been added to the 486 instruction set that permit software entry into SMM, as well as saving and restoring the total CPU state when in SMM mode.

1.5 Power Management

The ST486DX/DX2 power management features allow for a dramatic improvement in battery life over systems designed with non-static 486 processors. During suspend mode the typical current consumption is less than 1 percent of the full operation current.

Suspend mode is entered by either a hardware or a software initiated action. Using the hardware method to initiate suspend mode involves a two-pin handshake between the SUSP# and SUSPA# signals. The software can initiate suspend mode through the execution of the HALT instruction. Once in suspend mode, the ST486DX/DX2 power consumption is further reduced by stopping the external clock input. The resulting current draw is typically less than 500 µA. Since the ST486DX/DX2 is static, no internal data is lost when the clock is stopped.

1.6 Signal Summary

The ST486DX/DX2 signal set includes five cache interface signals, two coprocessor interface signals, two power management signals, and two system management mode signals.

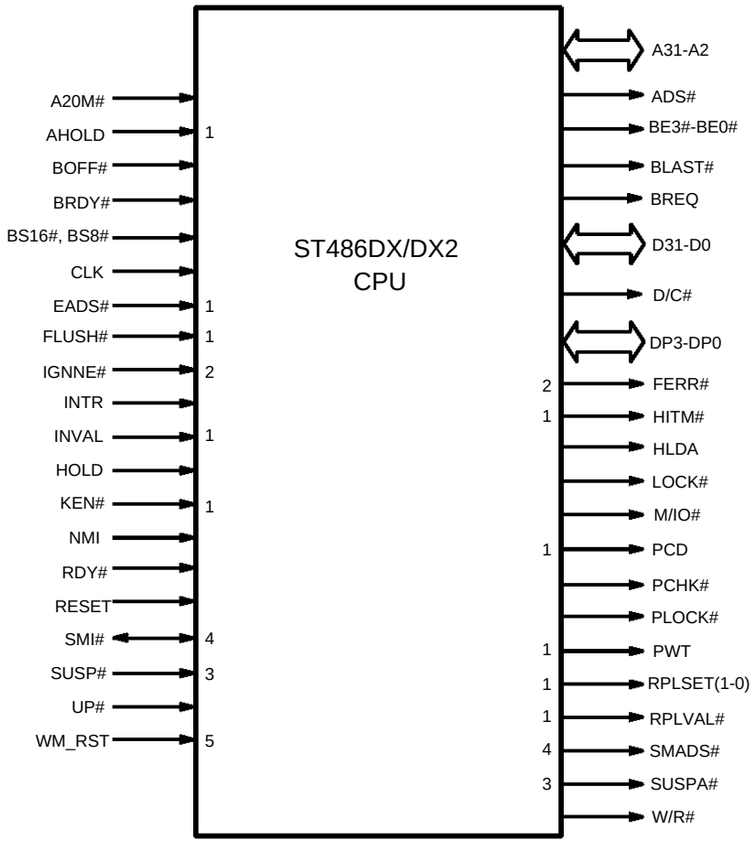


Figure 1 - 1.

2.0 ELECTRICAL SPECIFICATIONS

Electrical specifications in this chapter are valid for both the ST486DX and the clock-doubled ST486DX2. The ST486DX2 differs from the ST486DX in that the ST486DX2 internal CPU core operates at twice the frequency of the bus interface.

2.1 Electrical Connections

2.1.1 Power and Ground Connections and Decoupling

Due to the high frequency of operation of the ST486DX/DX2, it is necessary to install and test this device using standard high frequency techniques. The high clock frequencies used in the ST486DX/DX2 and its output buffer circuits can cause transient power surges when several output buffers switch output levels simultaneously. These effects can be minimized by filtering the DC power leads with low-inductance decoupling capacitors, using low impedance wiring, and by utilizing all of the VCC and GND pins.

2.1.2 Pull-Up/Pull-Down Resistors

Table 2-1 lists the input pins which are internally connected to pull-up and pull-down resistors. The pull-up resistors are connected to VCC and the pull-down resistors are connected to VSS. When unused, these inputs do not require connection to external pull-up or pull-down resistors. The SUSP# pin is unique in that it is connected to a pull-up resistor only when SUSP# is not asserted.

Table 2 - 1. Pins Connected to Internal Pull-Up and Pull-Down Resistors

SIGNAL	RESISTOR
A20M#	20-kΩ pull-up
AHOLD	20-kΩ pull-down
BOFF#	20-kΩ pull-up
BS16#	20-kΩ pull-up
BS8#	20-kΩ pull-up
BRDY#	20-kΩ pull-up
EADS#	20-kΩ pull-up
FLUSH#	20-kΩ pull-up
IGNNE#	20-kΩ pull-up
INVAL	20-kΩ pull-up
KEN#	20-kΩ pull-up
RDY#	20-kΩ pull-up
UP#	20-kΩ pull-up
SUSP#	20-kΩ pull-up
WM_RST	20-kΩ pull-down

It is recommended that the ADS#, LOCK# and SMI# output pins be connected to pull-up resistors, as indicated in Table 2-2. The external pull-ups guarantee that the signals remain negated during hold acknowledge states.

Table 2 - 2. Pins Requiring External Pull-Up Resistors

SIGNAL	EXTERNAL RESISTOR
ADS#	20-kΩ pull-up
LOCK#	20-kΩ pull-up
SMI#	20-kΩ pull-up

2.1.3 Unused Input Pins

All inputs not used by the system designer and not listed in Table 2-1 (Page 5) should be connected either to ground or to VCC. Connect active-high inputs to ground through a 20 kΩ (±10%) pull-down resistor and active-low inputs to VCC through a 20 kΩ (±10%) pull-up resistor to prevent possible spurious operation.

2.1.4 NC Designated Pins

Pins designated NC should be left disconnected. Connecting an NC pin to a pull-up resistor, pull-down resistor, or an active signal could cause unexpected results and possible circuit malfunctions.

2.2 Absolute Maximum Ratings

The following table lists absolute maximum ratings for the ST486DX/DX2 microprocessors. Stresses beyond those listed under Table 2-3 limits may cause permanent damage to the device. These are stress ratings only and do not imply that operation under any conditions other than those listed under "Recommended Operating Conditions" Table 2-4 (Page 6) is possible. Exposure to conditions beyond Table 2-3 may (1) reduce device reliability and (2) result in premature failure even when there is no immediately apparent sign of failure. Prolonged exposure to conditions at or near the absolute maximum ratings (Table 2-3) may also result in reduced useful life and reliability.

Table 2 - 3. Absolute Maximum Ratings

PARAMETER	ST486DX/DX2		UNITS	NOTES
	MIN	MAX		
Case Temperature	-65°	+110°	C	Power Applied
Storage Temperature	-65°	+150°	C	No Bias
Supply Voltage, VCC	-0.5	6.5	V	With Respect to V_{SS}
Voltage On Any Pin	-0.5	V_{CC} + 0.5	V	With Respect to V_{SS}
Input Clamp Current, I_{IK}		10	mA	Power Applied
Output Clamp Current, I_{OK}		25	mA	Power Applied

2.3 Recommended Operating Conditions

Table 2-4 presents the recommended operating conditions for the ST486DX/DX2 device.

Table 2 - 4. Recommended Operating Conditions

PARAMETER	ST486DX/DX2		UNITS	NOTES
	MIN	MAX		
T_C Case Temperature	0°	+85°	C	Power Applied
V_{CC} Supply Voltage	4.75	5.25	V	With Respect to Vss
V_{IH} High Level Input	2	V_{CC}+0.3	V	
V_{IL} Low Level Input	-0.3	0.8	V	
I_{OH} Output Current (High)		-1	mA	$V_{OH}=V_{OH(MIN)}$
I_{OL} Output Current (Low)		5	mA	$V_{OL}=V_{OL(MAX)}$

2.4 DC Characteristics

Table 2 - 5. DC Characteristics (at Recommended Operating Conditions)

PARAMETER	ST486DX/DX2		UNITS	NOTES
	MIN	MAX		
V_{OL} Output Low Voltage I_{OL} = 5 mA		0.45	V	
V_{OH} Output High Voltage I_{OH} = -1 mA	2.4		V	
I_{LI} Input Leakage Current For all pins except those listed in Table 2-1.		±15	µA	$0<V_{IN}<V_{CC}$
I_{IH} Input Leakage Current For all pins with internal pull-downs.		200	µA	V_{IH} = 2.4 V See Table 2-1.
I_{IL} Input Leakage Current For all pins with internal pull-ups		-400	µA	V_{IL} = 0.45 V See Table 2-1.
I_{CC} Active I_{CC} 33 MHz 40 MHz 50 MHz 66 MHz 80 MHz	Typical: 610 685 765 860 955	 925 1025 1170 1325 1575	mA	Note 1
I_{CCSM} Suspend Mode I_{CC} 33 MHz 40 MHz 50 MHz 66 MHz 80 MHz	Typical: 12.5 13.5 15.5 18 20	 24.5 27 31 35 39	mA	Note 1, 3
I_{CCSS} Standby I_{CC} 0 MHz (Suspended/CLK Stopped)	Typical: 0.45	 1.1	mA	Note 4
C_{IN} Input Capacitance		20	pF	f_c = 1 MHz (Note 2)
C_{OUT} Output or I/O Capacitance		20	pF	f_c = 1 MHz (Note 2)
C_{CLK} CLK Capacitance		20	pF	f_c = 1 MHz (Note 2)

Notes:
1. MHz ratings refer to internal clock frequency.
2. Not 100% tested.
3. All inputs at 0.4 or VCC - 0.4 (CMOS levels). All inputs held static except clock and all outputs unloaded (static IOUT = 0 mA). Specification also valid for UP# = 0.
4. All inputs at 0.4 or VCC - 0.4 (CMOS levels). All inputs held static and all outputs unloaded (static IOUT = 0 mA).

3.0 MECHANICAL SPECIFICATIONS

3.1 168-Pin PGA Package

The pin assignments for the ST486DX/DX2 168-pin PGA package are shown in Figure 3-1. The pins are listed by signal name and pin number in Table 3-2.

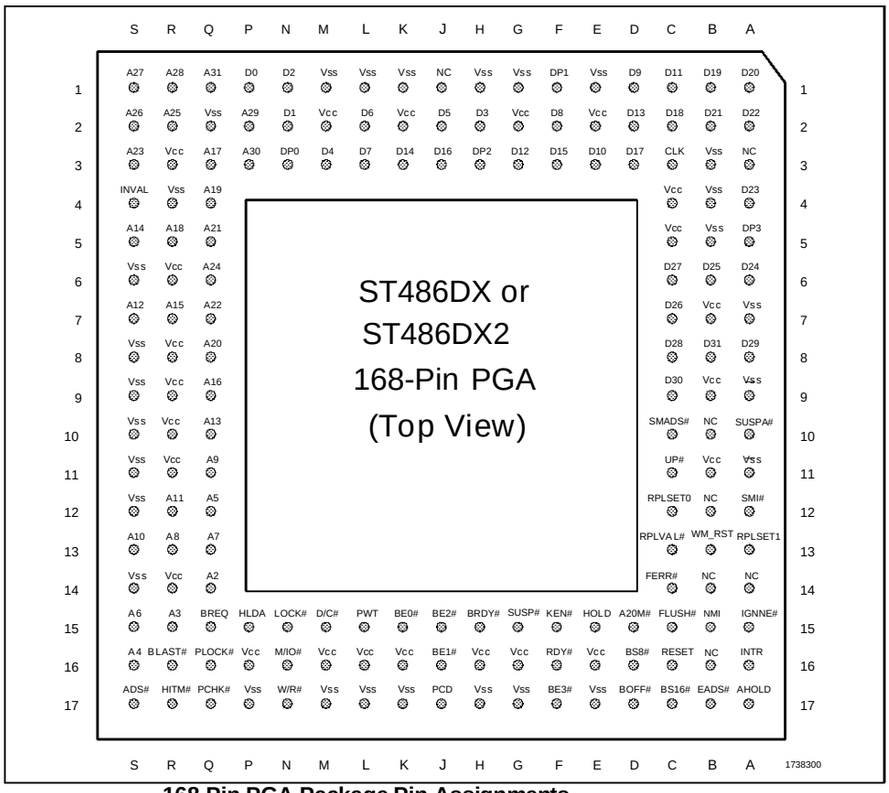


Figure 3 - 1. 168-Pin PGA Package Pin Assignments

Table 3 - 2. 168-Pin PGA Package Pin Numbers Sorted by Signal Name

Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.
A2	Q14	A29	P2	D11	C1	HITM#	R17	SUSP#	G15	VSS	A11
A3	R15	A30	P3	D12	G3	HLDA	P15	SUSPA#	A10	VSS	B3
A4	S16	A31	Q1	D13	D2	HOLD	E15	UP#	C11	VSS	B4
A5	Q12	ADS#	S17	D14	K3	IGNNE#	A15	VCC	B7	VSS	B5
A6	S15	AHOLD	A17	D15	F3	INTR	A16	VCC	B9	VSS	E1
A7	Q13	BE0#	K15	D16	J3	INVAL	S4	VCC	B11	VSS	E17
A8	R13	BE1#	J16	D17	D3	KEN#	F15	VCC	C4	VSS	G1
A9	Q11	BE2#	J15	D18	C2	LOCK#	N15	VCC	C5	VSS	G17
A10	S13	BE3#	F17	D19	B1	M/IO#	N16	VCC	E2	VSS	H1
A11	R12	BLAST#	R16	D20	A1	NC	A3	VCC	E16	VSS	H17
A12	S7	BOFF#	D17	D21	B2	NC	A14	VCC	G2	VSS	K1
A13	Q10	BRDY#	H15	D22	A2	NC	B10	VCC	G16	VSS	K17
A14	S5	BREQ	Q15	D23	A4	NC	B12	VCC	H16	VSS	L1
A15	R7	BS8#	D16	D24	A6	NC	B14	VCC	K2	VSS	L17
A16	Q9	BS16#	C17	D25	B6	NC	B16	VCC	K16	VSS	M1
A17	Q3	CLK	C3	D26	C7	NC	J1	VCC	L16	VSS	M17
A18	R5	D/C#	M15	D27	C6	NMI	B15	VCC	M2	VSS	P17
A19	Q4	D0	P1	D28	C8	PCD	J17	VCC	M16	VSS	Q2
A20	Q8	D1	N2	D29	A8	PCHK#	Q17	VCC	P16	VSS	R4
A20M#	D15	D2	N1	D30	C9	PLOCK#	Q16	VCC	R3	VSS	S6
A21	Q5	D3	H2	D31	B8	PWT	L15	VCC	R6	VSS	S8
A22	Q7	D4	M3	DP0	N3	RDY#	F16	VCC	R8	VSS	S9
A23	S3	D5	J2	DP1	F1	RESET	C16	VCC	R9	VSS	S10
A24	Q6	D6	L2	DP2	H3	RPLSET0	C12	VCC	R10	VSS	S11
A25	R2	D7	L3	DP3	A5	RPLSET1	A13	VCC	R11	VSS	S12
A26	S2	D8	F2	EADS#	B17	RPLVAL#	C13	VCC	R14	VSS	S14
A27	S1	D9	D1	FERR#	C14	SMADS#	C10	VSS	A7	W/R#	N17
A28	R1	D10	E3	FLUSH#	C15	SMI#	A12	VSS	A9	WM_RST	B13

3.3 Thermal Characteristics

The ST486DX/DX2 is designed to operate when case temperature is between 0° - 85°C. The case temperature is measured on the top center of the package. The maximum die temperature **($T_{J\ MAX}$)** and the maximum ambient temperature (T_{aMAX}) can be calculated using the following equations.

$$T_{j\ MAX} = T_c + (P_{MAX} \times \theta_{jc})$$

$$T_{a\ MAX} = T_j - (P_{MAX} \times \theta_{ja})$$

where:

$T_{j\ MAX}$ = Maximum average junction temperature (°C)

T_c = Case temperature at top center of package (°C)

P_{MAX} = Maximum device power dissipation (W)

θ_{jc} = Junction-to-case thermal resistance (°C/W)

$T_{a\ MAX}$ = Maximum ambient temperature (°C)

T_j = Average junction temperature (°C)

θ_{ja} = Junction-to-ambient thermal resistance (°C/W)

PGA Package

Table 3-3 lists the junction-to-ambient and junction-to-case thermal resistances for the PGA package. Table 3-4 lists the maximum ambient temperatures permitted for various clock frequencies and airflows for the PGA Package for Vcc equal to 5.25 volts. Package dimensions for the heatsink used for the thermal analysis are shown in Figure 3-2
(Page 11) and Table 3-5 (Page 11).

Table 3 - 3. PGA Package Thermal Resistance and Airflow

AIRFLOW (FT/MIN)	PGA THERMAL RESISTANCE (C/W)			
	WITH HEATSINK		WITHOUT HEATSINK	
	θja	θjc	θja	θjc
0	12	3.5	17	3.0
200	8	3.5	15	3.0
400	6	3.5	12	3.0
600	4.5	3.5	10	3.0
800	4	3.5	9	3.0

Table 3 - 4. PGA Package Maximum Ambient Temperature (T_A) with V_{CC} =5.25 V

CPU INTERNAL CLOCK FREQUENCY	HEATSINK	AIRFLOW				
		0 (FT/MIN)	200 (FT/MIN)	400 (FT/MIN)	600 (FT/MIN)	800 (FT/MIN)
33 MHz	No	17 °C	26 °C	41° C	51 °C	55° C
33 MHz	Yes	43° C	63 °C	73° C	80 °C	82 °C
40 MHz	Yes	39° C	60 °C	71° C	79 °C	82 °C
50 MHz	Yes	32° C	57° C	69 °C	78 °C	81 °C
66 MHz	Yes	26 °C	53° C	67 °C	78 °C	81° C
80 MHz	Yes	see note	see note	65 °C	77 °C	81 °C

Note: The ST486DX2-80 (80MHz) requires a minimum airflow of 400 (FT/MIN) for safe operation. Active heatsink (fan incorporated) is recommended

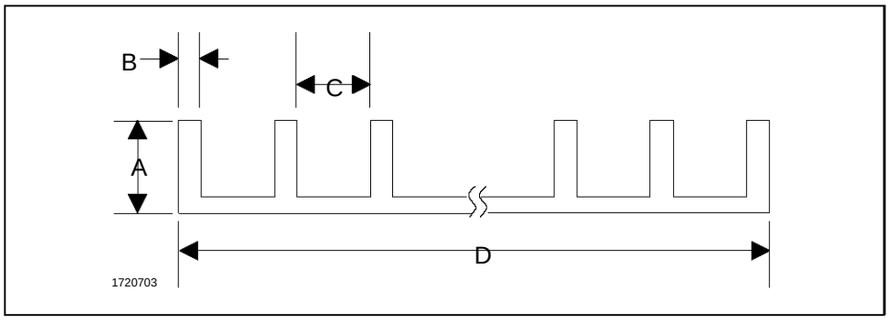
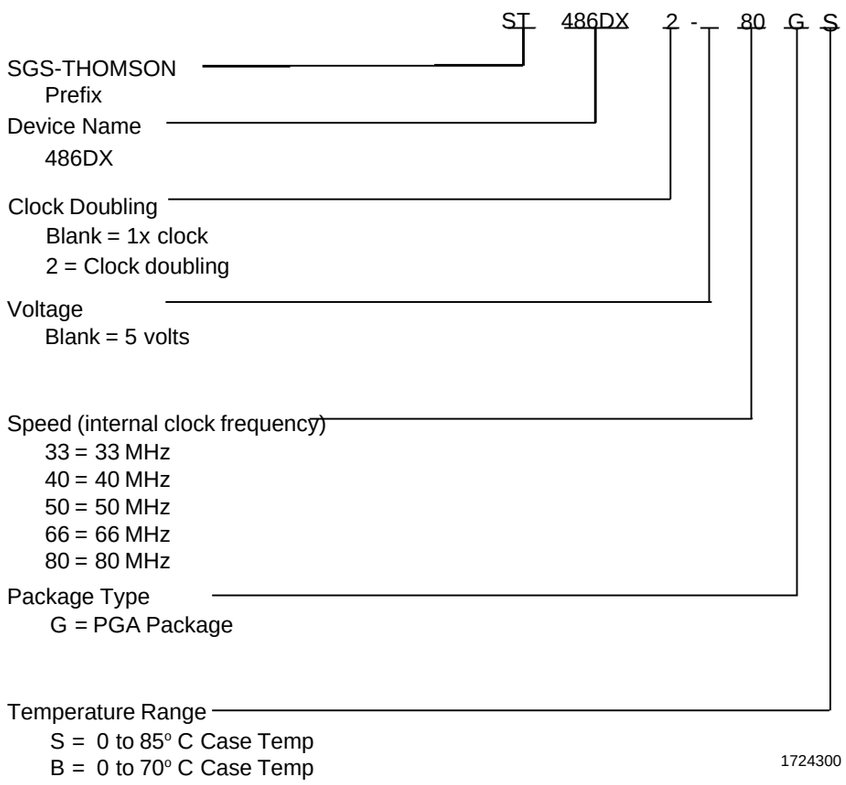


Figure 3 - 2. Heatsink for PGA Package

Table 3 - 5. Typical PGA Heatsink Dimensions

SYMBOL	MILLIMETERS	INCHES
A	6.1	0.24
B	1.3	0.05
C	4.8	0.19
D	39.1	1.54



To order the complete ST486DX/DX2 DATABOOK use order code: DBST486DXST/1

ST486DX and ST486DX2 Part Numbers

PART NUMBER	Vcc (V)	FREQUENCY (MHz)		PACKAGE
		BUS	INTERNAL	PGA
ST486DX-33GS	5.0	33	33	x
ST486DX-40GS	5.0	40	40	x
ST486DX-50GS	5.0	50	50	x
ST486DX2-50GS	5.0	25	50	x
ST486DX2-66GS	5.0	33	66	x
ST486DX2-80GS	5.0	40	80	x